Product Specification Sheet

TADDAX2Q58X-XXX

400G QSFP56-DD to 2x200G QSFP56 Active Optical Cable

Features

- Active optical cable with breakout from QSFP-DD 400G to two QSFP56 200G
- Up to 53.125Gbps data rate per channel by PAM4 modulation
- Integrated 850nm VCSEL array and PD array
- DDM function implemented
- Hot-pluggable
- Low power dissipation: <8W on QSFP-DD end, <4W on QSFP56 end
- Commercial operating case temperature range: 0℃ to 70 ℃
- Compliant with ROHS2.0

Applications

- Data centers and Cloud Networks

Standards

- IEEE 802.3cd
- CMIS4.0

Rev	Date	Modified by	Description
A	Nov 5,2021	Alan	Initial Release
B	Mar 3, 2022	Alan	Update 200G end mechanical outline

1. Absolute Maximum Ratings

Product	Electrical mode	Protocol	Nominal Rate			Specifications		Link
			Aggregate (Gbps)	Electrical Lanes(Gbaud)	ppm	High Speed Electrical	Pre-FEC Max BER	
QSFP-DD end	8X50	IEEE802.3cd	425	26.5625 PAM4	±100	400GAUI-8	2.4E-4	0.5~100m
QSFP56 end	4X50	IEEE802.3cd	212.5	26.5625 PAM4	±100	200GAUI-4	2.4E-4	

Parameter	Symbol	Unit	Min	Max
Case Operating Temperature	Top	℃	0	+70
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	0	85
Power Supply Voltage	Vcc	V	-0.5	+3.6

2. Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tca	°C	0	/	70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465

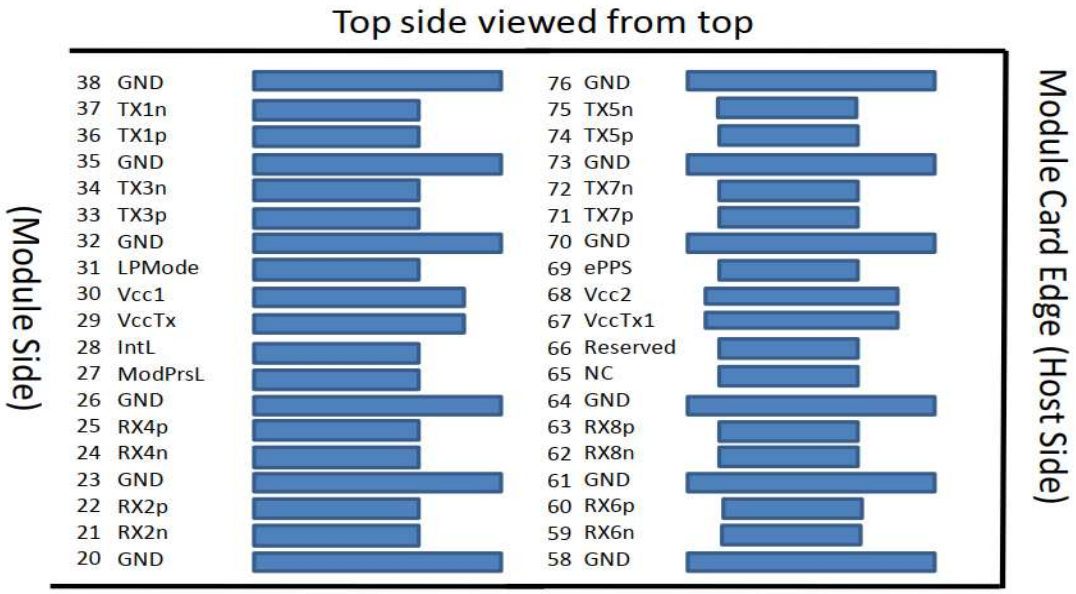
3. Electric Ports Definition

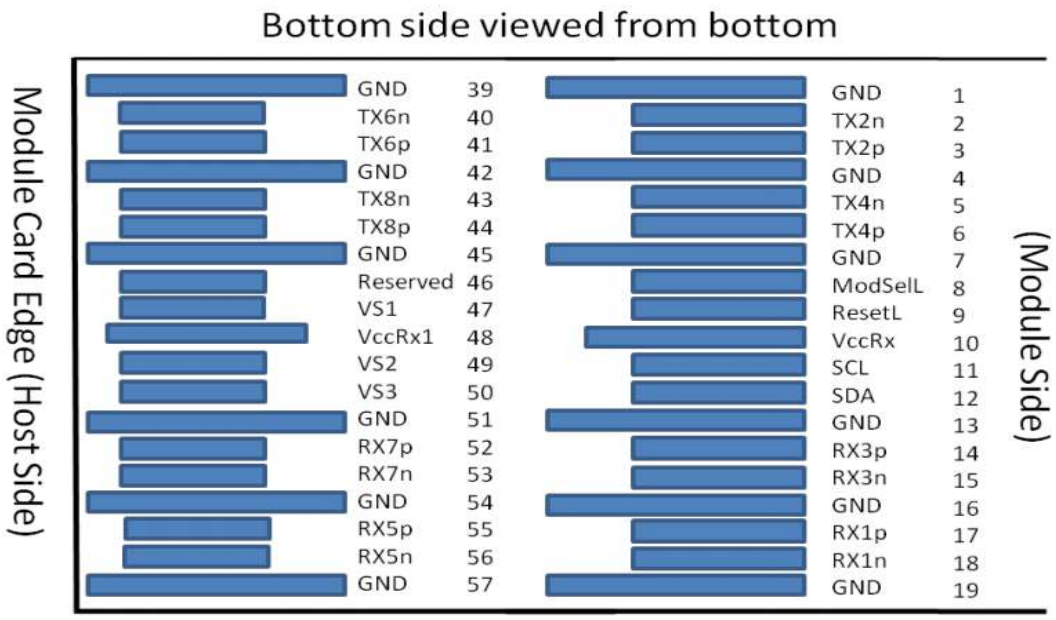
Parameter	Symbol	Unit	Min	Typ	Max	Notes
Supply Voltage	VCC	V	3.135	3.3	3.465	
Power Consumption	Pc	W			8	400G end
					4	200G end
Transmitter						
Input Differential Impedance	R_{IN}	Ω	80	100	120	
Single Ended Data Input Swing	V_{IN}	mVp-p	90		500	
Transmit Disable Voltage	V_{DIS}	V	2		V_{CCHOST}	
Transmit Enable Voltage	V_{EN}	V	V_{EE}		VEE+0.8	

Transmit Fault Assert Voltage	V_{FA}	V	2		V_{CCHOST}	
Transmit Fault De-Assert Voltage	V_{FDA}	V	V_{EE}		V_{EE}+0.8	
Receiver						
Single Ended Data Output Swing	V_{OD}	mVp-p	200		500	
LOS Fault	V_{LOSFT}	V	2		V_{CCHOST}	
LOS Normal	V_{LOSNR}	V	V_{EE}		V_{EE}+0.8	
Differential termination mismatch		%			10	
IIC communication						
IIC Clock frequency	-	KHZ	/	100	400	
clock stretching	-	us	/	/	500	

4. Pin Description

a. QSFP-DD end





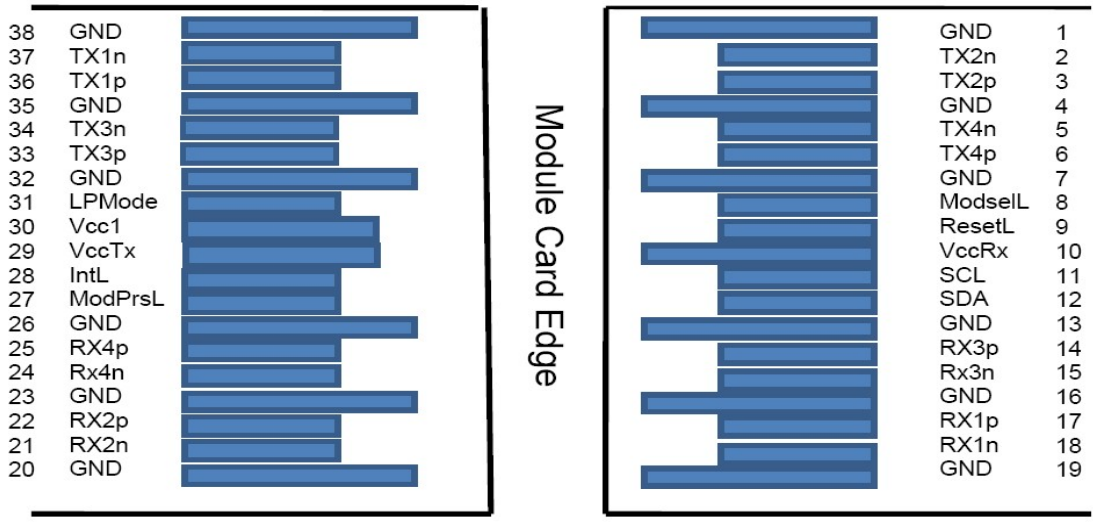
Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.

b. QSFP56 end

The electrical interface to the transceiver is a 38 pins edge connector. The 38 pins provide high speed data, low speed monitoring and control signals, I2C communication, power and ground connectivity. The top and bottom views of the connector are provided below, as well as a table outlining the contact numbering, symbol and full description.



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin	Symbol	Name/Description
1	GND	Ground
2	Tx2n	Transmitter Inverted Data Input
3	Tx2p	Transmitter Non-Inverted Data Input
4	GND	Ground
5	Tx4n	Transmitter Inverted Data Input
6	Tx4p	Transmitter Non-Inverted Data Input
7	GND	Ground
8	ModSelL	Module Select
9	ResetL	Module Reset
10	Vcc Rx	+3.3 V Power supply receiver
11	SCL	2-wire serial interface clock
12	SDA	2-wire serial interface data
13	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output
15	Rx3n	Receiver Inverted Data Output
16	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output

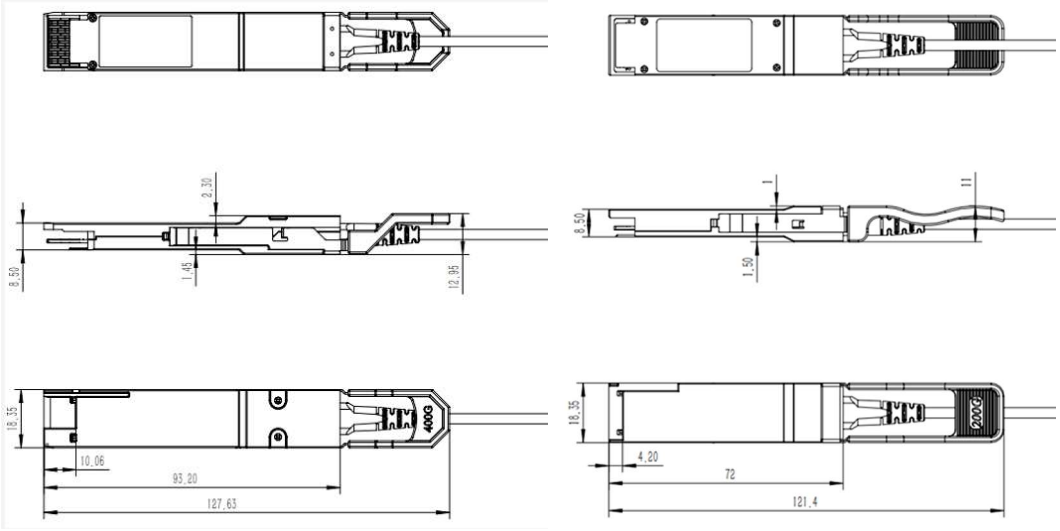
18	Rx1n	Receiver Inverted Data Output
19	GND	Ground
20	GND	Ground
21	Rx2n	Receiver Inverted Data Output
22	Rx2p	Receiver Non-Inverted Data Output
23	GND	Ground
24	Rx4n	Receiver Inverted Data Output
25	Rx4p	Receiver Non-Inverted Data Output
26	GND	Ground
27	ModPrsL	Module Present
28	IntL	Interrupt
29	Vcc Tx	+3.3 V Power supply transmitter
30	Vcc1	+3.3 V Power Supply
31	LPMode	Low Power Mode
32	GND	Ground
33	Tx3p	Transmitter Non-Inverted Data Input
34	Tx3n	Transmitter Inverted Data Input
35	GND	Ground
36	Tx1p	Transmitter Non-Inverted Data Input
37	Tx1n	Transmitter Inverted Data Input
38	GND	Ground

5. Module Memory Map

Compatible with CMIS rev 4.0

6. Package Outline

The mechanical specifications are based on QSFP-DD and QSFP56 transceiver module specification, substituting the optical connectors with a cable connecting both ends.



QSFP-DD end　　QSFP56 end

Cable Breakout point

Total Length（m）	Breakout * 2*200G(m)
1	0.5
2	0.5
3	1
5	2
7	3
10	3
X (X>10)	3

7. Standard Cable lengths for each PN

Part Number	Description
TADDAX2Q58X-001	400G QSFP56-DD SR8 AOC FanOut To 2*200G QSFP56 SR4 1M
TADDAX2Q58X-003	400G QSFP56-DD SR8 AOC FanOut To 2*200G QSFP56 SR4 3M
TADDAX2Q58X-005	400G QSFP56-DD SR8 AOC FanOut To 2*200G QSFP56 SR4 5M
TADDAX2Q58X-007	400G QSFP56-DD SR8 AOC FanOut To 2*200G QSFP56 SR4 7M
TADDAX2Q58X-010	400G QSFP56-DD SR8 AOC FanOut To 2*200G QSFP56 SR4 10M
TADDAX2Q58X-015	400G QSFP56-DD SR8 AOC FanOut To 2*200G QSFP56 SR4 15M
TADDAX2Q58X-020	400G QSFP56-DD SR8 AOC FanOut To 2*200G QSFP56 SR4 20M
TADDAX2Q58X-XXX	400G QSFP56-DD SR8 AOC FanOut To 2*200G QSFP56 SR4 xxM

XX: customized; 01 means Trustnuo standard product

xx：means cable length