Product Specification Sheet

TNDD8CAXA-CDXXX

400G QSFP-DD Active Optical Cable

Features

- Up to 53.125Gbps data rate per channel by PAM4 modulation
- Support 400GAUI-8 electrical interface
- Integrated 850nm VCSEL array and PD array
- DDM function implemented
- Hot-pluggable QSFP-DD form factor
- Single +3.3V power supply
- Compliant with ROHS2.0

Applications

- Data centers and Cloud Networks

Standards

- IEEE 802.3cd
- QSFP-DD MSA
- CMIS4.0

Rev	Date	Modified by	Description
A	Nov 5,2021	Alan	Initial Release

1. Absolute Maximum Ratings

Product	Electrical mode	Protocol	Nominal Rate			Specifications		Link
			Aggregate (Gbps)	Electrical Lanes(Gbaud)	ppm	High Speed Electrical	Pre-FEC Max BER	
400G-AOC	8X50	IEEE802.3cd	425	26.5625 PAM4	±100	400GAUI-8	2.4E-4	0.5~100m

Parameter	Symbol	Unit	Min	Max
Case Operating Temperature	Top	℃	0	+70
Storage Temperature Range	Ts	℃	-40	+85
Relative Humidity	RH	%	0	85
Power Supply Voltage	Vcc	V	-0.5	+3.6

2. Recommended Operating Conditions

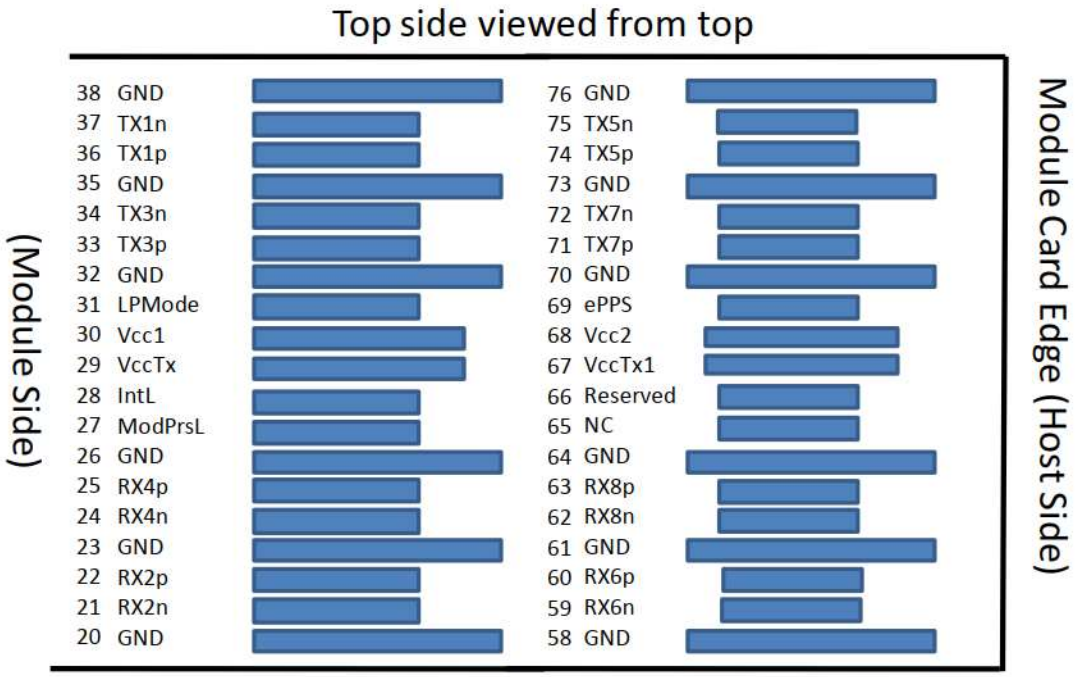
Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	Tca	°C	0	/	70
Power Supply Voltage	Vcc	V	3.135	3.3	3.465

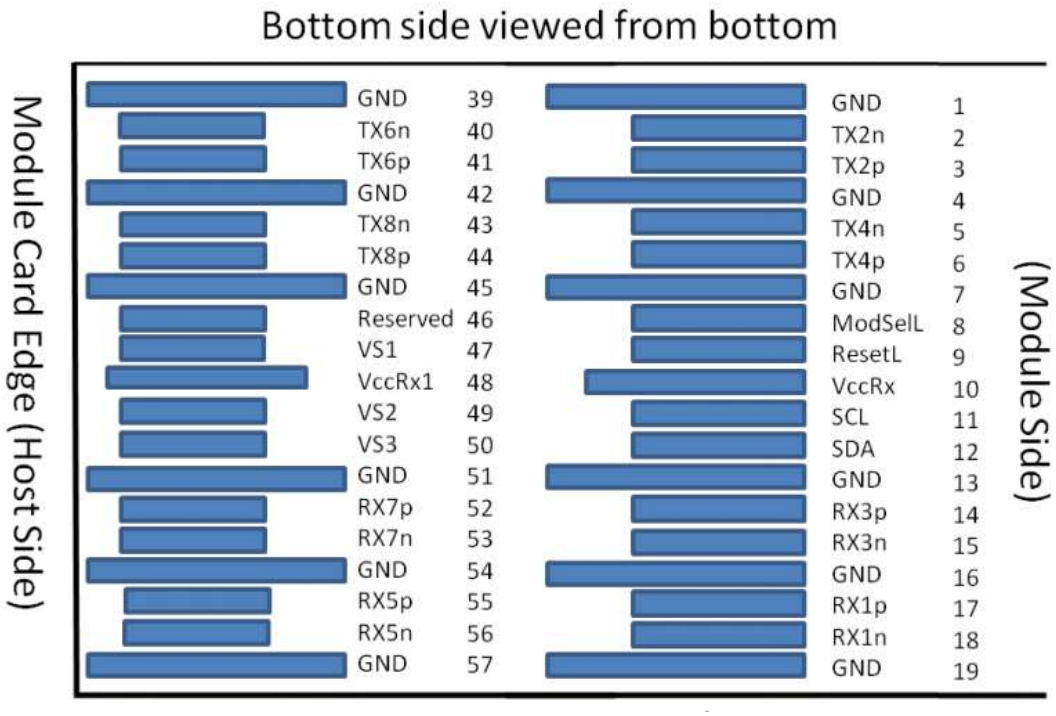
3. Electric Ports Definition

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Supply Voltage	VCC	V	3.135	3.3	3.465	
Power Consumption	Pc	W			8	per end
Transmitter						
Input Differential Impedance	R_{IN}	Ω	80	100	120	
Single Ended Data Input Swing	V_{IN}	mVp-p	90		500	
Transmit Disable Voltage	V_{DIS}	V	2		V_{CCHOST}	
Transmit Enable Voltage	V_{EN}	V	V_{EE}		VEE+0.8	
Transmit Fault Assert Voltage	V_{FA}	V	2		V_{CCHOST}	

Transmit Fault De-Assert Voltage	V_{FDA}	V	V_{EE}		V_{EE}+0.8	
Receiver						
Single Ended Data Output Swing	V_{OD}	mVp-p	200		500	
LOS Fault	V_{LOSFT}	V	2		V_{CCHOST}	
LOS Normal	V_{LOSNR}	V	V_{EE}		V_{EE}+0.8	
Differential termination mismatch		%			10	
IIC communication						
IIC Clock frequency	-	KHZ	/	100	400	
clock stretching	-	us	/	/	500	

4. Pin Description




Bottom side viewed from bottom
Module Card Edge (Host Side)
(Module Side)
GND 39
TX6n 40
TX6p 41
GND 42
TX8n 43
TX8p 44
GND 45
Reserved 46
VS1 47
VccRx1 48
VS2 49
VS3 50
GND 51
RX7p 52
RX7n 53
GND 54
RX5p 55
RX5n 56
GND 57
GND 1
TX2n 2
TX2p 3
GND 4
TX4n 5
TX4p 6
GND 7
ModSelL 8
ResetL 9
VccRx 10
SCL 11
SDA 12
GND 13
RX3p 14
RX3n 15
GND 16
RX1p 17
RX1n 18
GND 19

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

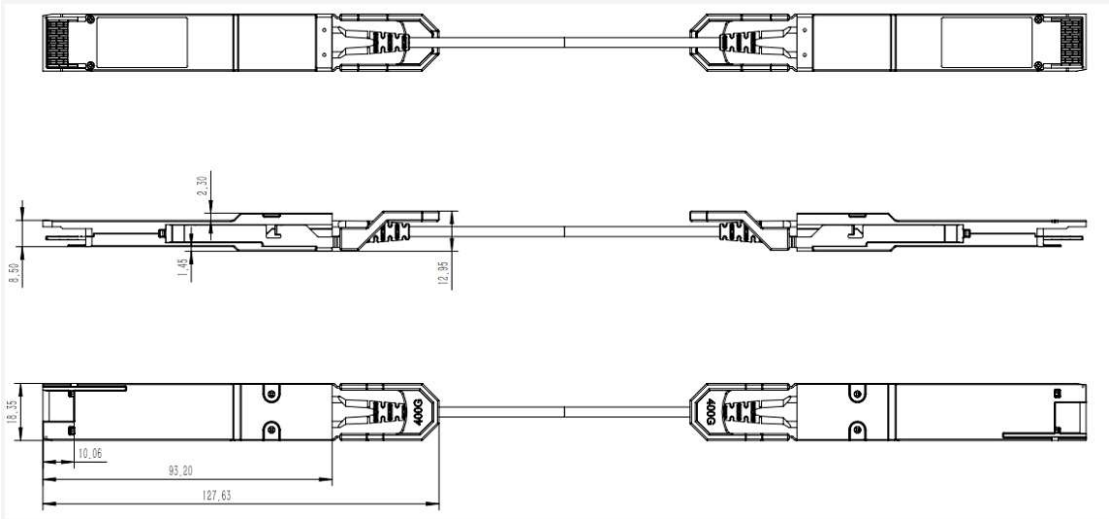
Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.

5. Module Memory Map

Compatible with QSFP-DD CMIS rev 4.0

6. Package Outline

Compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.



7. Standard Cable lengths for each PN

Part Number	Description
TNDD8CAXA-CD001	400G QSFP56-DD SR8 AOC 1M
TNDD8CAXA-CD003	400G QSFP56-DD SR8 AOC 3M
TNDD8CAXA-CD005	400G QSFP56-DD SR8 AOC 5M
TNDD8CAXA-CD007	400G QSFP56-DD SR8 AOC 7M
TNDD8CAXA-CD010	400G QSFP56-DD SR8 AOC 10M
TNDD8CAXA-CD015	400G QSFP56-DD SR8 AOC 15M
TNDD8CAXA-CD020	400G QSFP56-DD SR8 AOC 20M
TNDD8CAXA-CDXXX	400G QSFP56-DD SR8 AOC M

XX: customized; 01 means Trustnuo standard product

xx： means cable length